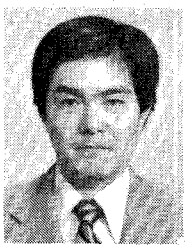


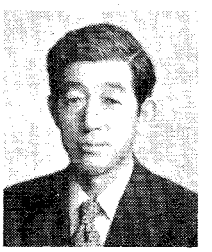
From 1975 to 1980 he was a Research Associate and from 1980 to 1983 he was a Lecturer in the Department of Electric Engineering, Ibaraki Technical College, Katsuta, Japan. He is now an Associate Professor. His research interests include circuit theory and matching network design.

Mr. Endo is a member of the Institute of Electronics and Communication Engineers of Japan.

Yoshiaki Nemoto (S'72–M'73) was born in Sendai City, Miyagiken, Japan, on December 2, 1945. He received the B.E., M.E., and Ph.D. degrees from Tohoku University, Sendai, Japan, in 1968, 1970, and 1973, respectively.

Since 1973 he has been a Research Associate with the Faculty of Engineering, Tohoku University. He has been engaged in research works in distributed networks and computer networks using satellites. He is co-recipient of the 1982 Microwave Prize from the IEEE Microwave Theory and Techniques Society.

Dr. Nemoto is a member of the Institute of Electronics and Communication Engineers of Japan.



Risaburo Sato (SM'62–F'77) was born in Furukawa City, Miyagiken, Japan, on September 23, 1921. He received the B.E. and the Ph.D. degrees from Tohoku University, Sendai, Japan, in 1944 and 1952, respectively.

From 1949 to 1961 he was an Assistant Professor at Tohoku University, and in 1961 he became a Professor in the Department of Electrical Communications at the same university. Since 1973 he has been a Professor in the Department of Information Science at Tohoku University. From 1969 to 1970 he was an International Research Fellow at Stanford Research Institute, Menlo Park, CA. His research activities include studies of multiconductor transmission systems, distributed transmission circuits, antennas, communication systems, active transmission lines, magnetic and ferroelectric recording, neural information processing, computer networks, and electromagnetic compatibility. He has published a number of technical papers and some books in these fields, including *Transmission Circuit*. He received the Paper Award from the Institute of Electrical Engineers of Japan (IEE of Japan) in 1955, the Kahoku Press Cultural Award in 1963, an award from the Invention Association of Japan in 1966, the Paper Award from the Institute of Electronics and Communication Engineers of Japan (IECE of Japan) in 1980, a Certificate of Appreciation of Electromagnetic Compatibility from the IEEE in 1981, and the Microwave Prize of the Microwave Theory and Techniques Society of IEEE in 1982.

Dr. Sato was the Vice President of IECE of Japan from 1974 to 1976. He has been a member of the Science Council of Japan from 1978 and a member of the Telecommunication Technology Consultative Committee at NTT from 1976. He is a chairman of EMC-S Tokyo Chapter of IEEE and a member of B.O.D. of EMC-S of IEEE. He is also a member of IECE of Japan, IEE of Japan, the Institute of Television Engineers of Japan, and the Information Processing Society of Japan.

High-Frequency Doubler Operation of GaAs Field-Effect Transistors

CHRISTEN RAUSCHER, SENIOR MEMBER, IEEE

Abstract—**A comprehensive study of single-gate GaAs FET frequency doublers is presented. Special emphasis is placed on exploring high-frequency limitations, while yielding explanations for previously observed lower frequency phenomena as well. Extensive large-signal simulations demonstrate the underlying relationships between circuit performance characteristics and principal design parameters. Verifying experiments include a straight frequency doubler and a self-oscillating doubler, both with output signal frequencies in *Ka*-band. The self-oscillating doubler appears especially attractive, yielding an overall dc-to-RF efficiency of 10 percent. The type of transistor employed in the numerical and experimental examples possesses a gate length of 0.5 μm and a gate width of 250 μm.**

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The author is with the Naval Research Laboratory, Washington, DC 20375.

I. Introduction

EFFORTS currently directed toward increased utilization of the millimeter-wave frequency range are providing a steady incentive to explore potential alternatives to existing means of generating RF power at these frequencies. In the solid-state domain, recent amplifier results indicate that GaAs FET's with subhalf-micron gate lengths are capable of attractive fundamental frequency oscillation up through at least 40 GHz. An appreciable extension in the useful frequency range for RF power generation should, in principle, be readily obtainable by exploiting device nonlinear properties that permit efficient frequency multi-

plication. Due to the particular nature of the device nonlinearities and the limitations imposed by parasitic effects at higher frequencies, the most promising mode of operation is that of frequency doubling. The objective of this study is to present a comprehensive analysis of GaAs FET frequency doublers aimed at establishing criteria for optimum circuit design.

Self-oscillating frequency doublers, in which the transistor functions both as fundamental frequency oscillator and second harmonic generator, warrant special attention. This type of circuit has the inherent ability to produce RF signal power at frequencies above those at which a given device would otherwise be considered for fundamental frequency oscillation. Based on capabilities of subhalf-micron devices [1], [2], and preliminary findings reported earlier [3], self-oscillating doubler circuits look promising for millimeter-wave operation. This is supported further by experimental results [4], [5] pertaining to generation of millimeter-wave power in the vicinity of 70 GHz, where half-micron gate length devices operating in a self-oscillating doubler mode have been used. Most of the previously published work on GaAs FET doublers [6]–[12], however, relates to nonoscillating doubler operation in the microwave range.

In contrast to the operation of power amplifiers and oscillators, which may be visualized as an essentially linear circuit problem perturbed by nonlinear effects, frequency multiplication relies specifically on nonlinear device behavior as the basic operating mechanism. Consequently, device-circuit interaction not only at the fundamental frequency, but also at the harmonic frequencies, is very crucial to the multiplication process. Although in the case of a frequency doubler it is mainly the fundamental frequency and its second harmonic to be concerned with, this still leaves transistor input *and* output impedance matching conditions at *both* these frequencies to be accounted for as potentially influential design considerations, in addition to the general dependence on drive level. Furthermore, as will be shown, device-external feedback options can play an important role, adding to the complexity of the overall problem. Due to the number of variables involved, it would be impractical to attempt to acquire comprehensive and conclusive information on GaAs FET frequency doubler operation solely on an experimental basis. Large-signal simulations are therefore employed as the principal means of analysis. By emphasizing highest frequency performance, device parasitic effects are accounted for under worst case conditions. This aids in identifying critical parasitic effects which can also have a large impact on doubler behavior at lower frequencies where such impact might not be readily expected. Experimental circuit realizations are subsequently used to verify the accuracy of the calculations and augment the predominantly experimentally based information reported previously in the literature [4]–[12]. The discussion deals with single-gate GaAs FET frequency doublers. But it should be noted that the basic conclusions to be drawn from this study apply to dual-gate GaAs FET circuits as well, provided—as is often the case—the dual-gate device is operating in a mode that permits it to be conceived as a cascade connection of two single-gate transistors, with one of them, in essence, engaged primarily in linear amplification.

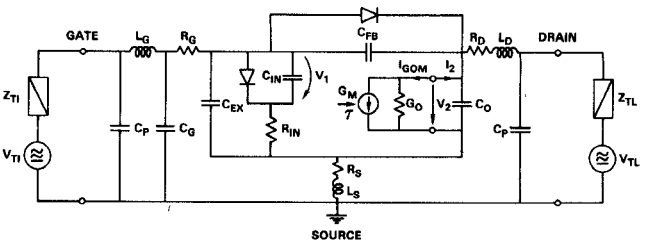

Fig. 1. GaAs FET equivalent circuit.

II. Approach to Large-Signal Simulation of GaAs FET Frequency Doublers

Efficient frequency doubling requires circuit elements with pronounced nonlinear characteristics for inflicting on an incoming fundamental frequency signal as much asymmetrical waveform distortion as possible while minimizing parasitic losses. With the prospect of overall conversion gain, GaAs FET's appear particularly attractive. The prominent nonlinearities in a GaAs FET [13], [14] are represented in the equivalent circuit of Fig. 1 by the voltage-dependent elements C_{IN}, R_{IN}, and C_{FB}, the two ideal diodes, the voltage-controlled current source at the output, and the associated voltage-dependent conductance G_O. Large-signal time-domain simulations carried out in connection with an earlier investigation [13] convey that the voltage dependences of C_{IN}, R_{IN}, and C_{FB} are relatively unattractive means through which to accomplish second harmonic generation. The same holds true for the output conductance G_O. The reason for this lies in the overshadowing prominence of transistor parasitic effects, especially those representing parasitic losses.

An effective way to employ a GaAs FET as a frequency doubler is to use it as a half-wave rectifier. This can be accomplished by operating the transistor either in the vicinity of forward conduction or in the vicinity of pinch-off. Measurements performed on a preliminary breadboard doubler circuit indicated that the two alternatives are roughly equivalent regarding fundamental to second harmonic frequency conversion efficiency. Operating in the vicinity of forward conduction actually appeared to provide approximately a one to two dB advantage, although no general conclusion should be drawn from this observation, as the opposite was found to be true in other situations [9]. Whatever the case, compared to operating around pinch-off, this involved higher dc drain current (and thus lower dc-to-RF efficiencies) as well as a higher risk of device failure due to elevated gate current spikes. Considering these drawbacks and their practical implications, the present study is directed toward investigating utilization of device pinch-off characteristics for frequency doubling.

To comprehensively assess large-signal GaAs FET

frequency doubler performance and still remain within reasonable computational bounds, it was necessary to develop a dedicated simulation program. In streamlining the numerical approach, only those nonlinearities were given full recognition which participate significantly in the frequency doubling process. Thus, with reference to the device equivalent circuit in Fig. 1, only the voltage-controlled current generator and the output conductance, which jointly describe the device intrinsic "dynamic" $I-V$ characteristics [14], need to be treated as full nonlinear elements. The less prominent nonlinearities—those associated with C_{IN}, R_{IN}, and C_{FB}— are represented by substituting *fixed* (linearized) large-signal time-average values for their respective voltage-dependent values. The action of the two diodes has been accounted for by limiting the positive voltage swings across them to +0.7 V. The diodes themselves are not included explicitly in order to bound the computational effort. Only the ability of the method to cope with *strongly* overdriven doubler operation, where forward conduction of the gate–source diode might become relevant, is compromised to some extent. But the overdriven case is of little practical relevance in the present context.

In deriving the equivalent circuit representation of a specific transistor, the voltage-independent values of its linear elements and the small-signal values of its various nonlinear elements are obtained from device S-parameter measurements with the help of standard curve-fitting techniques. The modeling effort is repeated for two or three representative bias voltage combinations in order to stake out the voltage dependence of the nonlinear elements. Assuming that characteristics of individual GaAs FET's exhibit a reasonable degree of similarity, the information contained in [13] and [14] can be scaled appropriately to yield estimates of element voltage dependence. As far as the elements C_{IN}, R_{IN}, and C_{FB} are concerned, these estimates formed the basis for determining their linearized, large-signal-equivalent values employed in the analysis. In the present context, trial computer runs were used to visualize the large-signal variations of the element values as a function of time. The variations were then subjected to straightforward arithmetic time-averaging. As the comparisons between predictions and experiments in Section IV demonstrate, there is little reason to question the appropriateness of this selective linearization.

As for the output nonlinear elements, they may be viewed as comprising a generalized controlled current source whose current $i_{GOM}(t)$ is expressed as a time-invariant function of voltages $v_1(t)$ and $v_2(t)$, and of time-delay τ (Fig. 1). The dynamic intrinsic device $I-V$ characteristics [14] described by this function are derived from the static (dc) $I_{DS}-V_{DS}$ characteristics by correcting them for the voltage drops across the drain and source parasitic series resistors and adjusting the slopes of the constant-input-voltage curves so as to conform with the small-signal values of the modeled output conductance G_O beyond the knees of the curves. The function $i_{GOM}(t)=$

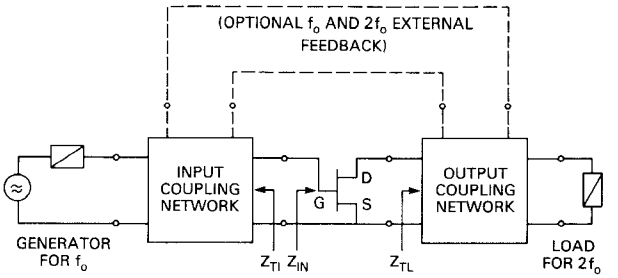

Fig. 2. GaAs FET frequency doubler.

$i_{GOM}[v_1(t-\tau), v_2(t)]$ was subsequently approximated by the following expression:

$$i_{GOM}[v_1(t-\tau), v_2(t)] = \{i_\alpha[v_1(t-\tau)] + [v_2(t) - V_{TL,0}] \cdot g_\alpha[v_1(t-\tau)]\}\{1-\exp[a\cdot v_2(t) + b\cdot v_2^2(t)]\} \quad (1)$$

with $V_{TL,0}$ the intrinsic drain–source bias voltage. The empirical relationships substituted for the terms $i_\alpha(v_1)$ and $g_\alpha(v_1)$ which, in principle, could assume varieties of forms, are

$$i_\alpha(v_1) = I_0 + I_1\cdot v_1 + I_2\cdot v_1^2 \quad (2)$$

and

$$g_\alpha(v_1) = \max\left\{\tilde{G}_O\cdot 1.3\cdot\sqrt{1-[v_1/V_p]}, \tilde{G}_{O\,\mathrm{sub}}\right\}. \quad (3)$$

The current component $i_\alpha(v_1)$ accounts for the major part of the v_1-dependence of i_{GOM}, with I_0 corresponding to I_{DSS} at the nominal drain–source bias voltage, and the coefficients I_1 and I_2 obtained through curve-fitting. The expression for $g_\alpha(v_1)$ approximates the output conductance variations with bias change, whereby $\tilde{G}_O$ represents the small-signal value of the output conductance G_O under nominal bias conditions, V_p designates the device pinch-off voltage, and $\tilde{G}_{O\,\mathrm{sub}}$ is the substrate leakage conductance. The approximations introduced here to describe $i_{GOM}[v_1(t-\tau), v_2(t)]$, again, appear to be more than adequate for practical purposes, as verified by the experimental results in Section IV.

The basic frequency doubler configuration is shown in Fig. 2, exhibiting a GaAs FET in common source configuration flanked by coupling networks which match the gate–source port of the device to the generator at the fundamental frequency and the device drain–source port to the external load at the second harmonic frequency. The numerical approach used in simulating large-signal frequency doubler performance relies on an adaptation of the harmonic balance technique in which the overall circuit is partitioned into a linear and a nonlinear subnetwork. This permits the major portion of the overall circuit to be treated conveniently in the frequency domain, while reserving time domain analysis for the nonlinear subcircuit. In the present case, the nonlinear part involves only the controlled current generator described by $i_{GOM}[v_1(t-\tau), v_2(t)]$, thus confining interaction between the subnetworks to the two output terminals of the current generator. The nonlinear solution is then sought by using computer optimization to force coincidence between the current $i_2(t)$

of the linear subnetwork and the current $i_{GOM}(t)$ of the nonlinear subnetwork, with the opposite sign applied to the latter (Fig. 1). The frequency-domain Fourier components of $v_2(t)$ are employed as optimization variables and serve both subnetworks as a common reference.

For the linear network portion, the task is to relate the voltage $v_2(t)$ to the intrinsic input voltage $v_1(t)$, needed subsequently for determining the nonlinear response $i_{GOM}[v_1(t-\tau), v_2(t)]$, and to the intrinsic load current $i_2(t)$. The analysis is formulated in terms of complex frequency-domain parameters denoted by capital letter symbols, with the supplementary index k referring to the harmonic number. The time-dependent quantities are approximated according to

$$v_1(t-\tau) = \sum_{k=0}^{N_f} \mathrm{Re}\{V_{1,k} \cdot e^{j2\pi k f_0 (t-\tau)}\} \tag{4}$$

$$v_2(t) = \sum_{k=0}^{N_f} \mathrm{Re}\{V_{2,k} \cdot e^{j2\pi k f_0 t}\} \tag{5}$$

$$i_2(t) = \sum_{k=0}^{N_f} \mathrm{Re}\{I_{2,k} \cdot e^{j2\pi k f_0 t}\} \tag{6}$$

as truncated Fourier series with up to N_f harmonics of the fundamental frequency f_0. This leads to sets of harmonic equations which relate the device-intrinsic frequency-domain voltage and current parameters, as defined in (4)–(6), to the device-external parameters imposed on the input and output ports of the transistor by the corresponding coupling networks. With reference to Fig. 1, the device-external parameters are represented by the equivalent port terminating impedances at each harmonic $Z_{TI,k}$ and $Z_{TL,k}$, $k = 0,1,2,\cdots$, and the associated equivalent port excitation voltages $V_{TI,k}$ and $V_{TL,k}$, $k = 0,1,2,\cdots$, with the subscript k again serving as abbreviated frequency indicator. Using symbols T and Y (with identifying subscripts) to denote *drive-level-independent* complex-variable voltage transfer ratios and transfer admittances, respectively, which are readily derived through straightforward circuit analysis using the superposition principle, the harmonic relationships assume the form

$$\begin{aligned} V_{1,k} = {} & V_{2,k} \cdot T_{21,k}(Z_{TI,k}, Z_{TL,k}) \\ & + V_{TI,k} \cdot T_{TI1,k}(Z_{TI,k}, Z_{TL,k}) \\ & + V_{TL,k} \cdot T_{TL1,k}(Z_{TI,k}, Z_{TL,k}), \\ & k = 0,1,2,\cdots \end{aligned} \tag{7}$$

$$\begin{aligned} I_{2,k} = {} & V_{2,k} \cdot Y_{22,k}(Z_{TI,k}, Z_{TL,k}) \\ & + V_{TI,k} \cdot Y_{TI2,k}(Z_{TI,k}, Z_{TL,k}) \\ & + V_{TL,k} \cdot Y_{TL2,k}(Z_{TI,k}, Z_{TL,k}), \\ & k = 0,1,2,\cdots. \end{aligned} \tag{8}$$

The excitation voltage components $V_{TI,0}$, $V_{TL,0}$, and $V_{TI,1}$ correspond to the gate–source bias voltage, the drain–source bias voltage, and the fundamental frequency excitation, respectively, with the rest of the excitation terms being zero. The voltage component $V_{TI,1}$, together with the equivalent terminating impedances at fundamental and second harmonic frequencies ($Z_{TI,k}$ and $Z_{TL,k}$, $k = 1,2$) are the crucial parameters whose bearing on doubler performance is the main subject of this study. Once (7) and (8) have been evaluated relative to $v_2(t)$, the results can then be applied to determining $i_{GOM}(t)$ using (1), (2), and (3).

In numerically carrying out the actual calculations, the respective voltages and currents are sampled by subdividing the fundamental frequency period into N_s equal time intervals Δt_s, yielding

$$v_1(p \cdot \Delta t_s - \tau) = \sum_{k=0}^{N_f} \mathrm{Re}\{V_{1,k} \cdot e^{j2\pi k(p/N_s - f_0 \cdot \tau)}\}, \quad p = 1,2,\cdots,N_s \tag{9}$$

$$v_2(p \cdot \Delta t_s) = \sum_{k=0}^{N_f} \mathrm{Re}\{V_{2,k} \cdot e^{j2\pi k p/N_s}\}, \quad p = 1,2,\cdots,N_s \tag{10}$$

$$i_2(p \cdot \Delta t_s) = \sum_{k=0}^{N_f} \mathrm{Re}\{I_{2,k} \cdot e^{j2\pi k p/N_s}\}, \quad p = 1,2,\cdots,N_s. \tag{11}$$

The overall solution is obtained by minimizing the least-square error function

$$E = \sum_{p=1}^{N_s} [i_{GOM}(v_1(p \cdot \Delta t_s - \tau), v_2(p \cdot \Delta t_s)) - i_2(p \cdot \Delta t_s)]^2 \tag{12}$$

with the help of a Levenberg-Marquardt routine [15], thereby utilizing the complex voltage components $V_{2,k}$, $k = 0,1,2,\cdots,N_f$ as the implicit optimization variables.

For the sake of uniformity, all results given in Section III are based on the assumption that the input port and the output port of the frequency doubler are conjugately matched at the fundamental frequency and second harmonic frequency, respectively. In order to determine the values of $Z_{TI,1}$ and $Z_{TL,2}$ representing these matching conditions, the large-signal equivalent values for the nonlinear transconductance G_M and output conductance G_O (Fig. 1) at both frequencies must be known. However, these values themselves depend on the final nonlinear network solution and are not available *a priori*. Various more or less sophisticated approximations were tried out. Results fully adequate for practical purposes were obtained with the very simplest procedure. This merely involves time-averaging over the fundamental frequency cycle of the voltage-dependent small-signal element values $\tilde{G}_M(v_1, v_2)$ and $\tilde{G}_O(v_1, v_2)$, to yield large-signal equivalent values, $\bar{G}_M$ and $\bar{G}_O$, according to

$$\begin{aligned} \bar{G}_{M,O} &= f_0 \cdot \int_0^{1/f_0} \tilde{G}_{M,O}[v_1(t-\tau), v_2(t)]\, dt \\ &\approx 1/N_s \cdot \sum_{p=1}^{N_S} \tilde{G}_{M,O}[v_1(p \cdot \Delta t_s - \tau), v_2(p \cdot \Delta t_s)]. \end{aligned} \tag{13}$$

These approximations, which are constantly updated as the calculations progress, are utilized in an iterative search for the optimum matching conditions. Each matching condition involves two variables, namely, the real part and the imaginary part of the respective impedance. By referring the matching problem to the intrinsic ports of the device, however, it is possible to reduce the number of variables in each search to only *one*. This is crucial to the practicability of the overall simulation effort because every discrete solution obtained during one of these searches involves in itself a nonlinear function minimization process pertaining to expression (12).

The program is set up to handle ten harmonics. As for the higher harmonic matching conditions, it is assumed throughout the calculation that

$$Z_{TI,k} = Z_{TL,k} = 0, \qquad k > 3. \tag{14}$$

These impedances play only minor roles in establishing frequency doubler operation so that the assumptions concerning them, introduced here for convenience, are of little practical consequence.

III. Large-Signal Frequency Doubler Simulation Results

A. The Basic Concept

The circuit configuration most commonly associated with GaAs FET frequency doublers is depicted in Fig. 2. The topology resembles that of an amplifier circuit. Indeed, impedance matching conditions and feedback options involve gain-bandwidth considerations analogous to those in amplifier designs, except that input and output now relate to different frequencies. Emphasis in the present context is on studying operation of the basic building block, namely, the doubler circuit which does not incorporate deliberate *external* feedback. Among the independent parameters impacting doubler performance, the three most relevant ones are focused on specifically: the fundamental frequency drive level, the device output terminating impedance at the fundamental frequency $Z_{TL}(f_0)$, and the device input terminating impedance at the second harmonic $Z_{TI}(2f_0)$. (In the previous section, the two impedance quantities had been respectively labeled $Z_{TL,1}$ and $Z_{TI,1}$ for the sake of brevity.) In accordance with intuition and confirming analysis, only *reactive* values for these terminating impedances need be considered, as any losses associated with them invariably will lead to suboptimal conversion efficiencies. Again as mentioned earlier, the device input at the fundamental frequency and the device output at the second harmonic frequency are always chosen to be optimally matched, thereby covering the most relevant situations and also providing a unified basis for comparing results.

One of the aspects of GaAs FET doublers to be highlighted later in this section relates to the significance of parasitic feedback within the transistor. The logical extension of this is to incorporate additional *external* feedback as indicated in Fig. 2 for counteracting or enhancing the parasitic feedback effects, depending on application. Carrying this notion one step further then leads to the self-oscillating frequency doubler circuit indicated in Fig. 3, whereby enough fundamental frequency feedback of appropriate kind is added externally to yield oscillation.

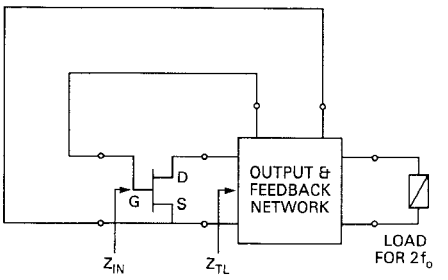

Fig. 3. Self-oscillating frequency doubler.

The type of transistor employed in the following numerical and experimental examples is the Avantek M106 GaAs FET which possesses a gate length of 0.5 μm and a gate width of 250 μm. The dc-bias condition common to all calculations comprises a drain–source voltage of +3.0 V and a gate–source voltage of −1.2 V, relative to a pinch-off voltage of −1.5 V. The gate bias voltage roughly corresponds to the point where the second derivative of drain current versus gate voltage, and thus second harmonic generation for low drive levels, is maximum. Due to the costs involved in carrying out large-signal simulations, consideration has been limited to this one particular set of bias voltages, representing a case judged to be of primary practical relevance. From the information compiled in this study and from published experimental results [9], the impact of bias voltage changes on doubler performance can be adequately assessed.

B. Dependence of Doubler Performance on Fundamental Frequency Output Termination and Input Drive Level

A first set of simulation results obtained with the program outlined in Section II is given in Fig. 4. The diagram depicts large-signal conversion efficiency as a function of second harmonic output power and fundamental frequency reactive load impedance $Z_{TL}(f_0)$. For plotting convenience later on, this reactance is expressed in terms of parameter θ according to $Z_{TL}(f_0) = j50\ \Omega \cdot \tan(\theta)$, whereby θ may be visualized as the electrical length of a fictitious short-circuited 50-Ω transmission line stub. The input frequency is 15 GHz, from which the second harmonic is derived at 30 GHz. A short circuit as the input is arbitrarily assumed for the second harmonic.

The two noteworthy observations to be derived from Fig. 4 are a) the dramatic dependence of RF conversion gain on fundamental frequency load reactance, and b) the relatively invariant values of maximum achievable second harmonic output power. The issue regarding the conversion gain variability is whether *nonlinear* device circuit interaction is indeed responsible for the phenomenon. The question is approached by conceptually separating nonlinear circuit effects from linear ones. This is achieved by substituting *fixed* large-signal equivalent values for each of the

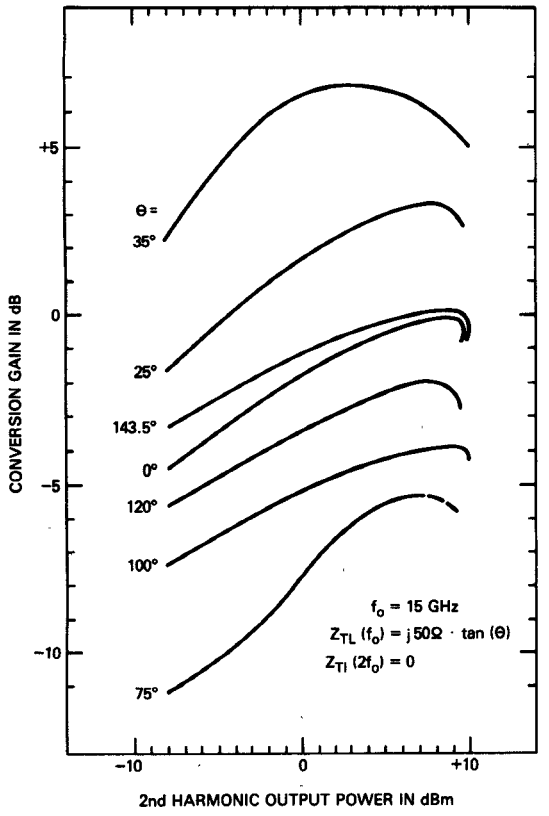

Fig. 4. Simulated large-signal conversion gain as a function of fundamental frequency load reactance $Z_{TL}(f_0)$ and second harmonic output power.

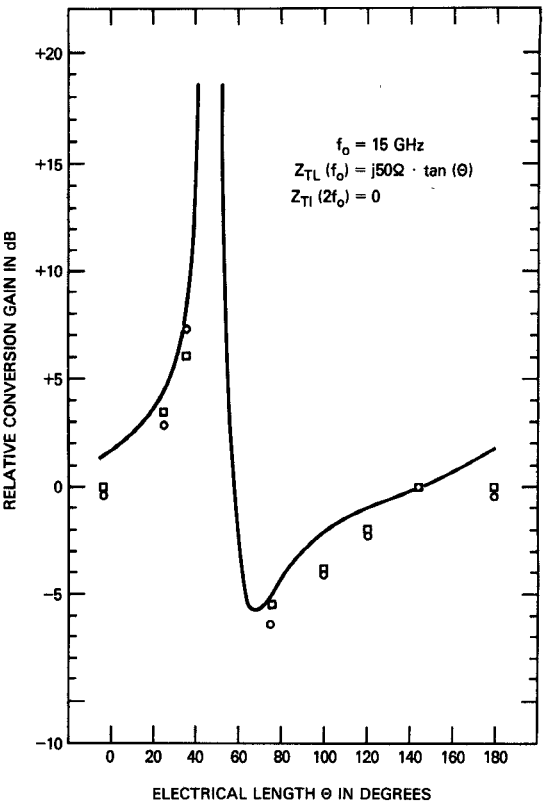

Fig. 5. Normalized conversion gain as a function of fundamental frequency load reactance parameter θ, comparing calculated large-signal results with the response of the linearized circuit. —— response of linearized circuit; ∘ ∘ ∘ large-signal response for an output power level of 0 dBm at 30 GHz; □□□ large-signal response for an output power level of 8 dBm at 30 GHz.

nonlinear elements in Fig. 1, including those related to $i_{GOM}(v_1, v_2)$, and then comparing transfer characteristics of the fully linearized circuit with those derived for nonlinear operation. The transfer function used to represent the linearized network is the ratio of the amplitude of the (fundamental frequency) voltage $v_1(t)$ and the incident power level. Fig. 5 shows the comparison between this transfer ratio and large-signal conversion gain values extracted from Fig. 4 for arbitrarily selected output power levels of 0 dBm and 8 dBm, respectively. The data is plotted as a function of fundamental frequency load reactance in terms of θ. To facilitate comparison, all values are normalized so as to coincide at $\theta = 143.5°$. This reference point, also chosen arbitrarily, represents the specific case of a fundamental frequency series resonance at the intrinsic drain–source port of the device.

Inherently, the transfer function calculated for the fully linearized circuit would be expected to show appreciable correlation with the large-signal conversion gain response as a result of the intrinsic voltage $v_1(t)$ being intimately associated with modulating device transconductance and with generating thereby the major portion of the second harmonic signal. The convincing degree of correlation demonstrated in Fig. 5 leads to the conclusion that the observed dependence of conversion gain on fundamental frequency load reactance is basically a linear circuit effect. This effect is specifically linked to parasitic feedback within the transistor, giving rise to conversion gain values that shoot off towards infinity as instability is approached at the fundamental frequency. In analogy to amplifier circuits it must be recognized, however, that conversion gain advantages sought through utilization of any kind of feedback mechanism are achieved at the expense of signal bandwidth. To illustrate this, fundamental frequency input impedance and corresponding input Q-factor have been calculated relative to the external gate–source port of the transistor (Fig. 2). They have been plotted in Fig. 6 against load reactance parameter θ for comparison with the results in Fig. 5.

Referring back to Fig. 4, the fundamental frequency feedback issue does not appear to noticeably influence maximum available output power level at the second harmonic. This is a direct consequence of the close coupling between the matched second harmonic load and the drain–source nonlinear controlled current generator (Fig. 1) engaged in frequency multiplication. Still, the commented output power invariance appears remarkable when related to the considerable changes the $i_{GOM} - v_2$ trajectories undergo as the fundamental frequency load reactance is varied. A representative sampling of these trajectories is given in Fig. 7.

C. Influence of Second Harmonic Input Termination and Feedback on Doubler Performance

The second harmonic frequencies under consideration lie beyond the frequency range of normal transistor operation.

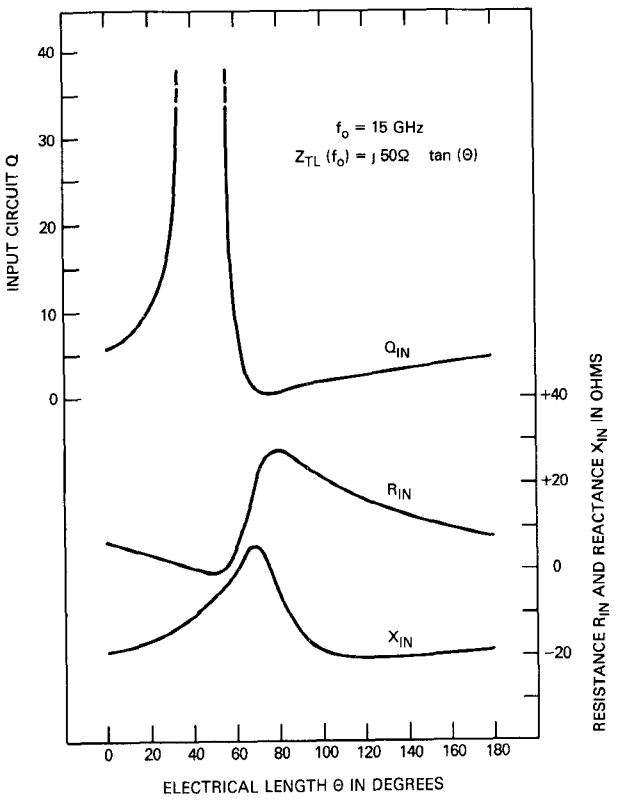

Fig. 6. Fundamental frequency input Q-factor Q_{IN} and input impedance $R_{IN} + jX_{IN}$ as a function of fundamental frequency load parameter θ.

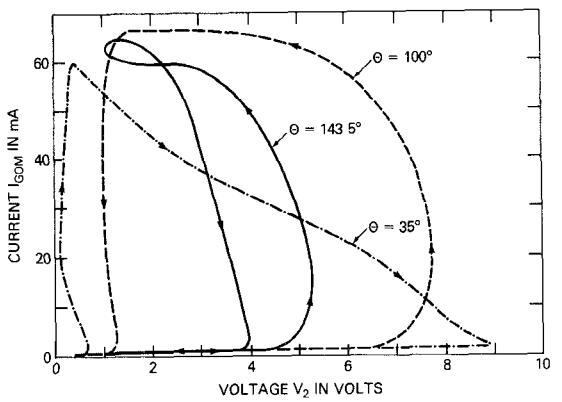

Fig. 7. Dynamic current-voltage trajectories in the i_{GOM}–v_2-plane for different fundamental frequency output load reactance values, with $Z_{TL}(f_0) = j50\ \Omega \cdot \tan(\theta)$ and $f_0 = 15$ GHz.

Parasitic feedback at the second harmonic assumes, thereby, a prominent role, causing the reactive input terminating impedance $Z_{TI}(2f_0) = jX_{TI}(2f_0)$ to become significantly involved in determining overall doubler performance. This is illustrated in the upper portion of Fig. 8, where large-signal conversion gain is plotted against input reactance $X_{TI}(2f_0)$. To avoid having to include drive level as an additional independent parameter, only *maximum achievable* conversion gain values are given for each particular value of $X_{TI}(2f_0)$. The input frequency of 18 GHz has been selected to accentuate the severity of the feedback problem

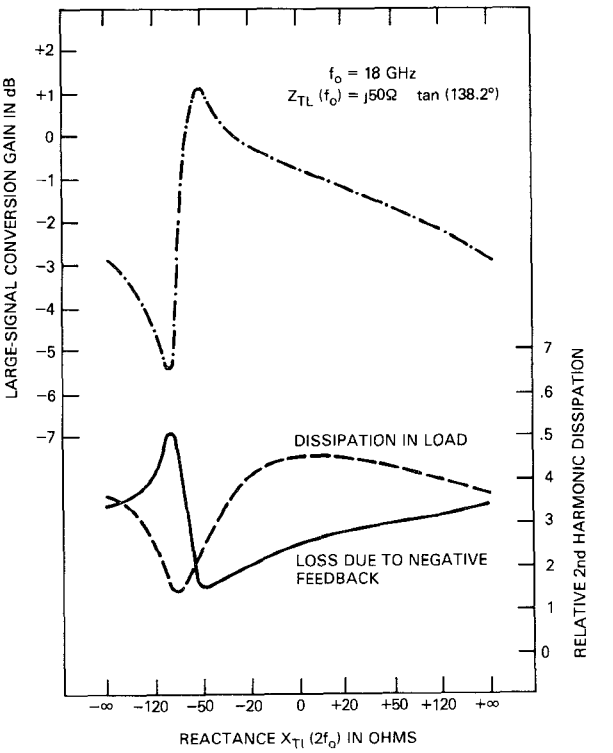

Fig. 8. Simulated maximum achievable large-signal conversion gain and corresponding components of second harmonic power dissipation as functions of second harmonic input terminating reactance $X_{TI}(2f_0)$.

at elevated second harmonic frequencies, as is demonstrated by the conspicuous resonant behavior of the conversion gain curve. The fundamental frequency reactive load impedance $Z_{TL}(f_0)$, with $\theta = 138.2°$, has been chosen to portray, again, a series resonant condition at the intrinsic drain–source port of the device.

To better understand how the pronounced variation in conversion gain comes about, it is revealing to investigate what fraction of the total second harmonic power generated in the nonlinear controlled source of the device equivalent circuit (Fig. 1) actually reaches the external load. This fraction has been calculated and is represented in the lower portion of Fig. 8 by the dashed curve. The superimposed solid-line curve refers to the fraction of power lost due to second harmonic signal fed via the input back to the intrinsic device output, where it gives rise to destructive interference. The third category of second harmonic loss contributions, namely, those attributed to the various parasitic resistances in the transistor, have not been plotted explicitly, but are given by the difference between unity and the sum of the other two contributions. As is readily observed by inspection of Fig. 8, the second harmonic feedback losses can be quite detrimental and are primarily responsible for the large dip in conversion gain. The conclusion drawn from this is that the proper choice of second harmonic input terminating reactance can be crucial.

The role of the second harmonic input reactance is de-emphasized as the operating frequency decreases. This is illustrated in the lower portion of Fig. 9 where conversion gain curves are plotted for three different fundamental

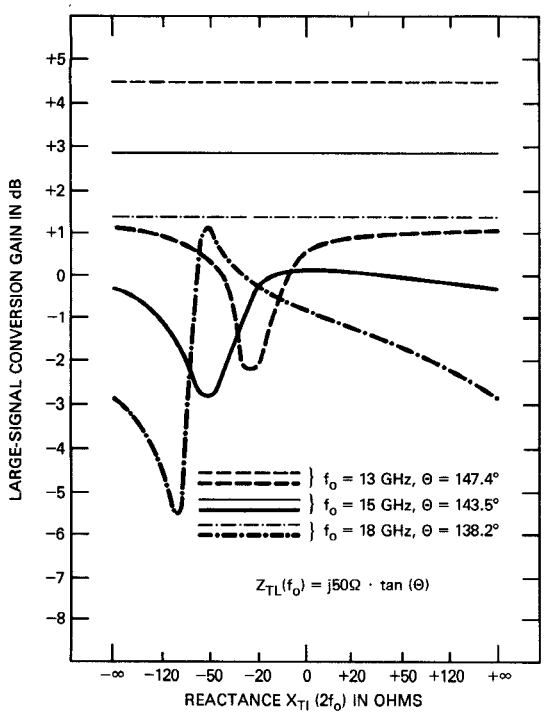

Fig. 9. Simulated maximum achievable large-signal conversion gain as a function of second harmonic input terminating reactance $X_{TI}(2f_0)$ for incident signals at 13 GHz, 15 GHz, and 18 GHz. The three bottom curves represent doubler performance without additional external feedback, whereas the three straight lines indicate achievable performance with appropriate external feedback applied to eliminate second harmonic parasitic feedback losses.

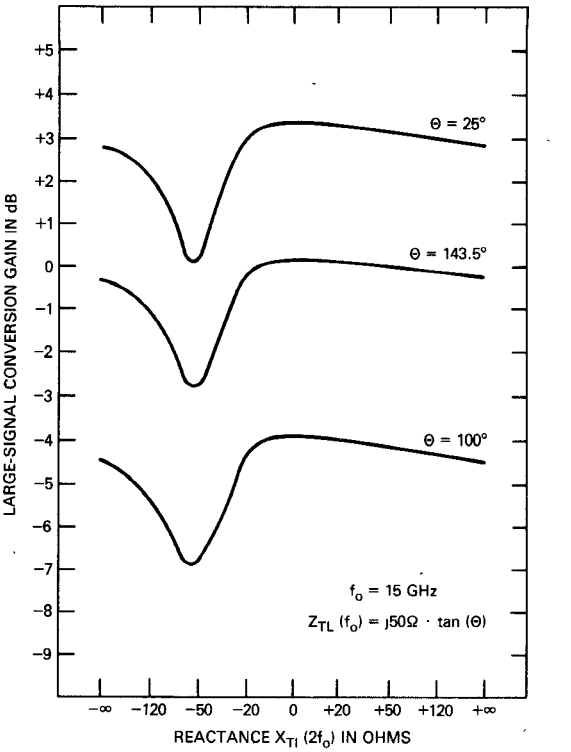

Fig. 10. Calculated maximum achievable large-signal conversion gain as a function of second harmonic input terminating reactance $X_{TI}(2f_0)$ and fundamental frequency load reactance parameter θ.

frequencies, for which series-resonated intrinsic outputs are assumed in each case. It should be noted, nevertheless, that even at the lowest of the three frequencies, the effects of destructive feedback interference are still quite appreciable. A direct way of addressing the basic problem is to institute additional external feedback at the second harmonic to counteract parasitic feedback. The three straight lines in the upper portion of Fig. 9 visualize the improvements in conversion gain to be obtained by incorporating feedback of proper amplitude and phase so as to cancel out the destructive intrinsic feedback effects. However, implementation of such a scheme only pays off if the transistor exhibits gain at the second harmonic. Thus, as is evident from Fig. 9, the most significant improvement is achievable at the lowest frequency, whereas at the highest frequency the reward is rather minor due to the fact that the transistor is running out of gain at 36 GHz. If sufficient second harmonic transistor gain is available, especially in lower frequency examples, most any RF-to-RF conversion gain value could be obtained as conditions for oscillation are approached. The actual use of second harmonic feedback will depend on the application, as it involves a direct trade-off among conversion gain, bandwidth, and circuit complexity. One obvious application is the fixed-tuned self-oscillating frequency doubler, where emphasis is on efficiency and where bandwidth is of no concern. An example of this type of circuit is given in Section IV.

Finally, Fig. 10 depicts conversion gain as a function of second harmonic input termination for different values of fundamental frequency (15 GHz) output reactance expressed in terms of parameter θ. The variation with θ corresponds to the behavior observed in Fig. 4. What is interesting here is that the shape of the curves in Fig. 10 appears to be essentially invariant to changes in θ. This implies, in effect, that device-circuit interaction at the fundamental frequency and interaction at the second harmonic are, to a good approximation, separable phenomena. They can thus be addressed independently, which translates into a significant asset when it comes to carrying out an actual design.

IV. Experimental Verification of Predicted Results

A. A 15-to-30-GHz Frequency Doubler

The GaAs FET frequency doubler shown in Fig. 11, which is implemented in microstrip on a 0.125-mm thick glass-fiber-reinforced teflon substrate, is specifically designed to offer verifiable circuit conditions that provide a sound experimental basis for establishing confidence in the analytical predictions of Section III. In support of this goal, the particular Avantek M106 transistor chip used in the experiment was selected to reflect, as closely as possible, the modeled device characteristics on which all simulation results in Section III have been based. Also, the bias voltages were kept the same, with $V_{GS} = -1.2$ V and $V_{DS} = +3.0$ V. Only a single transistor in common source configuration is used in order to avoid any potential com-

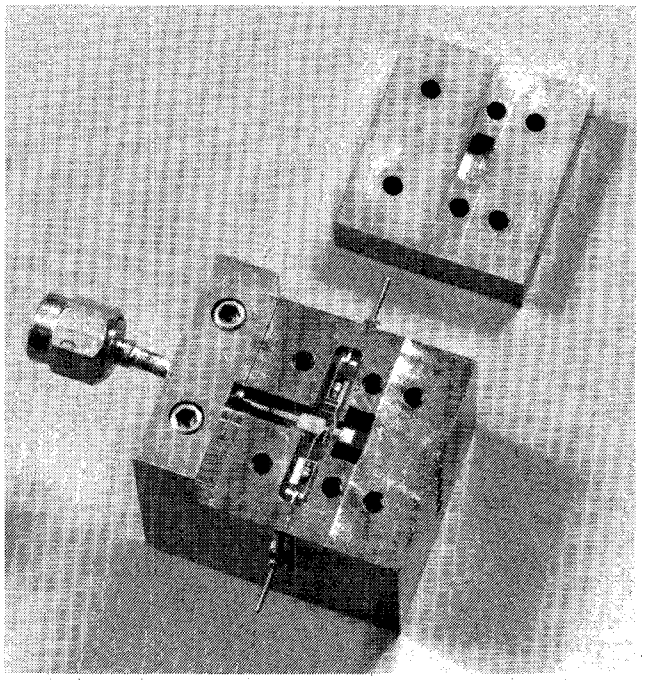

Fig. 11. GaAs FET 15-to-30 GHz frequency doubler, using an Avantek M106 transistor biased at $V_{GS} = -1.2$ V and $V_{DS} = +3.0$ V.

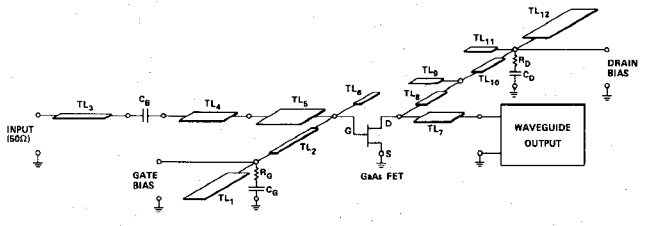

Fig. 12. Schematic circuit diagram of the 15-to-30 GHz frequency doubler. The various *TL* elements represent microstrip transmission lines.

bining efficiency problems like those experienced in a previously reported balanced *Ka*-band oscillator-doubler circuit [3].

A schematic of the experimental doubler circuit is given in Fig. 12. Apart from the components associated with the gate bias circuitry (R_G, C_G, TL_1, and TL_2), the input coupling network consists of a cascade of impedance transforming transmission-line elements (TL_3, TL_4, and TL_5), a dc blocking capacitor (C_B), and an open-circuited stub (TL_6) which is a quarter of a wavelength long at 30 GHz. They provide a conjugate match for the incident 15-GHz fundamental frequency signal and simultaneously block the second harmonic by short-circuiting the gate port of the FET at 30 GHz. The generated second harmonic output power is probe-coupled via a short piece of transmission line (TL_7) to a section of *Ka*-band waveguide with backshort. The probe and its associated stray capacitances act as an open-circuited stub at the fundamental frequency, thereby establishing a reactive load with an effective value for the parameter θ defined in Section III of $\theta = 135°$. The drain bias circuitry (R_D, C_D, and TL_8 through TL_{12}) connected to the probe is designed to reject both the 15-GHz and the 30-GHz signals. No deliberate external

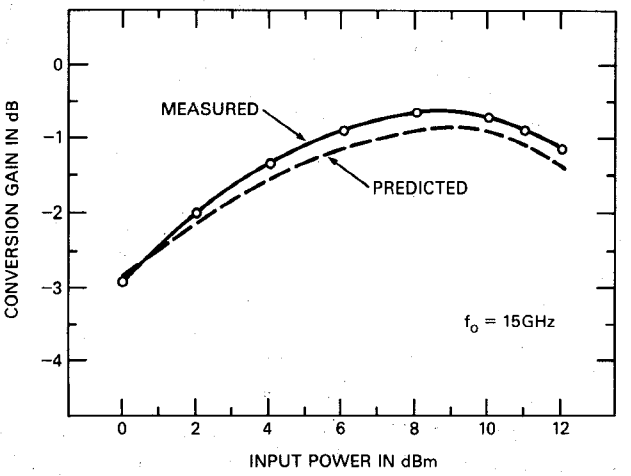

Fig. 13. Measured and predicted performance of 15-to-30 GHz frequency doubler circuit.

feedback is applied at either the fundamental or the second harmonic frequency.

Large-signal simulations were carried out to predict performance characteristics of this particular doubler configuration. A comparison between the calculated results and the measured response is given in Fig. 13. Care was taken to accurately account for parasitics associated with the mounting of the transistor and with the probe coupling, helping to achieve, presumably, the good agreement between theory and experiment. Nevertheless, to obtain this agreement, it was necessary to allow some trimming of the circuit in order to compensate for unavoidable inaccuracies in assessing parasitic effects at 30 GHz. In anticipation of this need, three tuning screws were incorporated in the *Ka*-band waveguide section.

A circuit of this kind has the potential of being relatively broadband. Using standard frequency domain analysis, bandwidth capabilities may be readily estimated based on input and output matching constraints at the pertinent frequencies. Although straightforward, bandwidth was not studied explicitly in this context because of the inherent limitation imposed on the verifying experiment by appreciable transistor lead reactance values at 30 GHz. These reactance values were dictated by the relatively long gate and drain bond wires, whose minimum lengths were determined by what could be comfortably accommodated with available device mounting techniques. To optimize bandwidth at the elevated output frequencies considered here, it is necessary to not only reduce dominating parasitics as much as possible, but also to select the best topology. Balanced configurations are especially attractive. Their principal merit lies, ideally, in decoupling input and output signals through symmetry, hence bypassing limitations otherwise imposed by the necessity to achieve signal separation through filtering.

B. A Ka-Band Self-Oscillating Frequency Doubler

The verifying experiment described in this subsection involves a signal generator that relies on a single GaAs

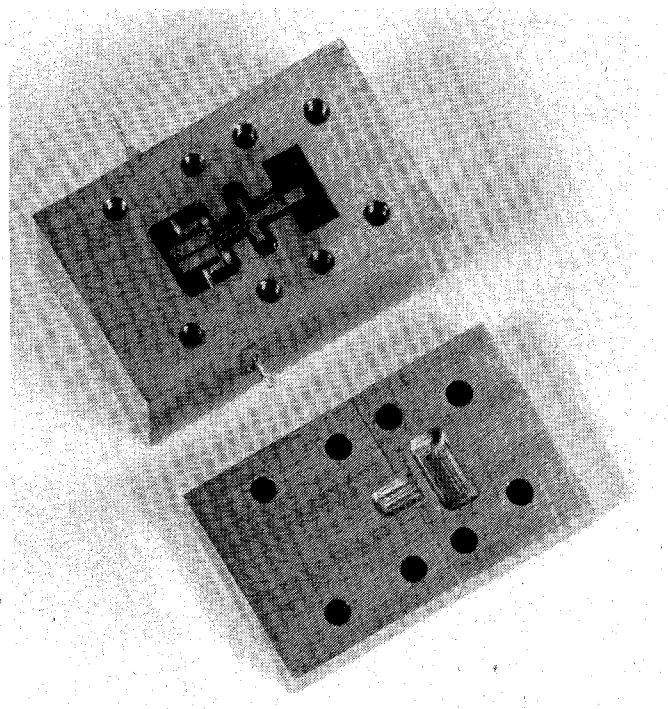

Fig. 14. Self-oscillating GaAs FET frequency doubler providing an overall dc-to-RF conversion efficiency of 10 percent in *Ka*-band.

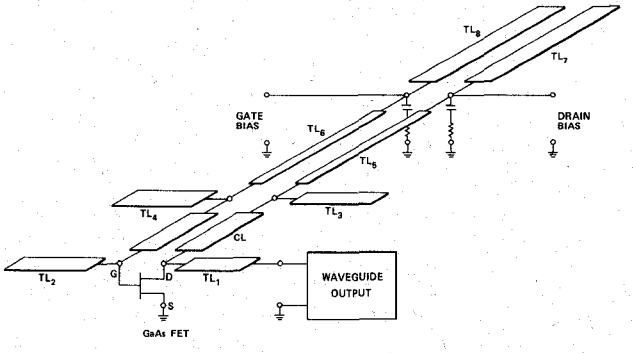

Fig. 15. Schematic circuit diagram of the *Ka*-band self-oscillating frequency doubler, with the *TL* elements representing microstrip transmission lines.

FET to deliver second harmonic power at *Ka*-band to an external load, while sustaining fundamental frequency oscillation at *Ku*-band. This example complements the one discussed in the previous subsection by highlighting the external feedback option. The actual circuit, realized in microstrip on a 0.25-mm glass-fiber-reinforced teflon substrate, is depicted in Fig. 14. The employed transistor is, again, a carefully selected Avantek M106 chip, whose characteristics closely resemble those assumed in the simulations. As illustrated by the schematic of the circuit given in Fig. 15, the output and feedback network referred to in Fig. 3 consists of a probe which reactively terminates the fundamental frequency signal and couples the second harmonic output power to a backshorted *Ka*-band waveguide section, and of a composite feedback network. The latter contains a pair of parallel coupled lines (*CL*), augmented by transmission line stubs (TL_2, TL_3, and TL_4), thereby providing proper oscillation conditions at the fundamental frequency as well as optimum feedback at the second harmonic. Gate and drain bias circuitry (TL_5 through TL_8, and two *RC* elements) form an integral part.

In connection with Fig. 10 (Section III), it was pointed out that—aside from the principal second harmonic generation process—device-circuit interaction at the fundamental frequency and at the second harmonic could be viewed as largely independent phenomena. This observation was exploited in designing the self-oscillating doubler, as it allowed the fundamental frequency oscillation problem to be treated separately from the optimization of second harmonic output power. As for the oscillation conditions, they differ from those generally associated with conventional GaAs FET oscillators by not having to supply fundamental frequency power to an external load. As a series of supplementary simulations have shown, highest dc-to-RF conversion efficiencies are obtained when the intrinsic drain–source current i_{GOM} (Fig. 1) is fully modulated without yet incurring appreciable waveform clipping as the gate–source voltage goes positive. Taking this into account, the fundamental frequency portion of the self-oscillating doubler design is merely a special case among the more general situations treated earlier [16], which permits available computational tools to be readily adapted and put to work for the current task. Following determination of drive level and circuit conditions at the fundamental frequency, optimization of conditions at the second harmonic is then pursued in accordance with procedures developed in Section III.

The experimental circuit was designed to provide 9.1 dBm of output power at 30 GHz with an overall dc-to-RF conversion efficiency of 9.1 percent. The nominal bias voltages, as in all previous examples, were $V_{GS} = -1.2$ V and $V_{DS} = +3.0$ V. With small-signal device transconductance being approximately half its maximum value, this provides sufficient gain to accomplish stable fundamental frequency oscillation while offering efficient frequency multiplication. The measured performance compared favorably with the predictions, yielding 8.8 dBm of output power at 29.34 GHz with 8.9-percent efficiency. To achieve these results, it was again necessary to compensate for various uncertainties regarding parasitic effects at 30 GHz by trimming one of the microstrip transmission line stubs and tweaking the output with the help of tuning screws provided in the output waveguide section.

To gain additional information and to satisfy curiosity, the reaction of the test circuit to changes in gate bias voltage was investigated experimentally. The results are summarized in Figs. 16 and 17, together with the predictions for the nominal bias point. As would be expected, the indicated responses of second harmonic output power, dc-to-RF efficiency, dc drain current, and output frequency all show some variation with gate bias. Efficiency peaked at 10 percent. However, the interesting thing to note here is how small these variations actually are when compared to the wide range of gate bias voltages, starting close to pinch-off and running all the way up to 0 V. The insensitiv-

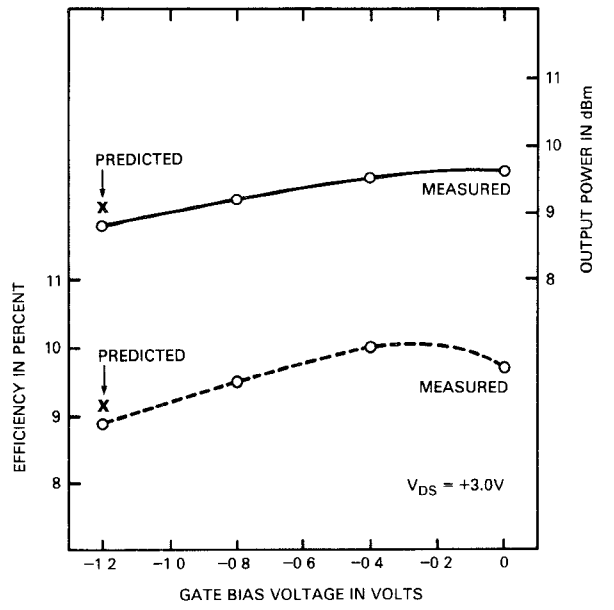

Fig 16. Second harmonic output power and dc-to-RF efficiency as a function of gate–source bias voltage for the self-oscillating frequency doubler. —— measured output power; ----- measured dc-to-RF efficiency; and x 30-GHz performance predictions for the nominal gate-source bias voltage of $V_{GS} = -1.2$ V.

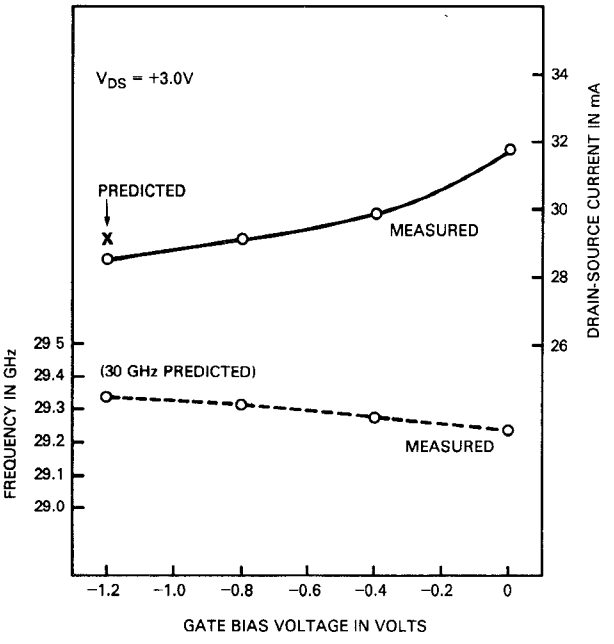

Fig. 17. DC drain–source current and output frequency as a function of gate–source bias voltage for the self-oscillating doubler. —— measured dc drain–source current; ----- measured output frequency; and x predicted dc drain–source current for 30 GHz operation with the transistor biased at the nominal gate–source bias voltage of $V_{GS} = -1.2$ V.

ity to gate bias is believed to result from signal clamping effects related to the composite action of the gate–source Schottky-barrier diode and the associated input capacitances.

V. Conclusions

An extensive treatment of single-gate GaAs FET frequency doublers has been described, focusing on modulation of transistor pinch-off characteristics as the primary multiplying mechanism. This mode of operation is believed to be preferable to other alternatives when it comes to achieving performance while guarding device reliability. Besides offering a comprehensive set of simulation results relative to a variety of different circuit parameter combinations, the study has, above all, demonstrated the important role that device-internal parasitic feedback plays in determining doubler performance. It has also been shown how additional external feedback can be utilized to improve RF conversion efficiency at the cost of bandwidth.

The principal experiments used for verification include a basic GaAs FET frequency doubler circuit and a self-oscillating doubler, both with output signal frequencies in *Ka*-band. The high degree of correlation observed between predictions and measurements provides reassurance regarding the practical relevance of the simulation results compiled in the present study. Emphasis has been, throughout, on extracting RF signal power from GaAs FET's at frequencies higher than those generally associated with conventional device operation. The basic conclusions naturally apply to less extreme situations at lower frequencies as well. Among the different types of circuits, the self-oscillating doubler looks particularly attractive, having yielded 10 percent dc-to-RF efficiency at around 30 GHz using a commercially available half-micron gate length device.

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Christen Rauscher (S'73–M'75–SM'81) was born in Boston, MA, on November 4, 1944. He received the diploma in electrical engineering and the Ph.D. degree in 1969 and 1975, respectively, both from the Swiss Federal Institute of Technology, Zurich, Switzerland.

From 1969 to 1976 he was employed as an Assistant and Research Associate at the Microwave Laboratory of the Swiss Federal Institute of Technology where he conducted research on computer-aided tolerance optimization of microwave active circuits and on IMPATT power amplifiers. He held a Postdoctoral Fellowship from the Swiss National Science foundation from 1976 to 1978. He spent this time at Cornell University, Ithaca, NY and the Naval Research Laboratory, Washington, DC, investigating the nonlinear behavior of GaAs MESFET's. Since 1978 he has been employed at the Naval Research Laboratory, Washington, DC, engaged in research on microwave and millimeter-wave nonlinear circuits.

Design and Analysis of the Channel Waveguide Transformer

PETER H. SIEGEL, STUDENT MEMBER, IEEE, DORN W. PETERSON, MEMBER, IEEE, AND ANTHONY R. KERR, SENIOR MEMBER, IEEE

Abstract—**The authors describe an easily fabricated *H*-plane transformer for use in rectangular waveguide carrying the dominant mode. An approximate theoretical analysis of the structure is presented, and computed results are compared with measurements on transformers at *X*-band. Design curves are given for transitions from full to one-half, one-third, and one-quarter height waveguide. The new transformers have been found particularly useful for millimeter-wave mixers and multipliers employing split-block construction. The structure can also be used as a transition from rectangular to channel waveguide.**

I. Introduction

WAVEGUIDE MIXERS and frequency multipliers often use reduced height waveguide for improved impedance matching to the nonlinear element. A stepped or tapered transformer is generally employed between the full and reduced height sections to minimize the mismatch. These transformers are especially difficult to fabricate at millimeter wavelengths where the guide dimensions are very small. Copper electroforming has been used successfully; however this process is time-consuming and usually requires the production of a disposable mandrel for each finished piece.

This paper describes a new form of *H*-plane transformer, particularly suitable for use in split-block rectangular waveguide, which can be made quickly and easily with a slitting saw or single-point cutting tool. The transformer has been used successfully in frequency doublers up to 220 GHz, and in mixers operating at 115 GHz.

A physical description of the transformer and detailed fabrication procedures are given in Section II. Section III outlines an approximate theoretical analysis for the determination of the reflection coefficient. The accuracy of the analysis is considered in Section IV where VSWR measurements of three *X*-band transformers are compared with computed values. In Section V, the theory is applied to two transformer configurations and design curves are given for transitions from full to one-half, one-third, and one-quarter height waveguide. Finally, in Section VI, two modifications are described which increase the bandwidth of the transformer.

II. Description of the Transformer

The channel waveguide transformer is shown in Fig. 1. It is most easily fabricated as a split-block structure in which the two halves are joined along a plane of zero transverse current (Fig. 1(d)). A slitting saw or single-point tool is used to cut the reduced height waveguide completely along the two blocks (Fig. 1(a)). The full height waveguide and transition region are then formed by moving the saw to each side of the centerline, producing a sloping channel in part of the block (Fig. 1(b) and (c)). The result is a length

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P. H. Siegel is with the Department of Electrical Engineering, Columbia University, New York, NY 10027.
D. W. Peterson is with the Department of Astronomy, Columbia University, New York, NY 10027.
A. R. Kerr is with the NASA/Goddard Institute for Space Studies, New York, NY 10025.

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